APPENDIX B

VERSION WITH MARKINGS TO SHOW CHANGES MADE
37 C.F.R. § 1.121(b)(iii) AND (c)(ii)

CLAIMS:

1. (Twice Amended) A trench-type power MOSFET having a vertical invertible channel composed of N type [one of the] conductivity material and [types] disposed between a source region and a drain region; a gate oxide and gate contact thereon extending along the length of said invertible channel and operable to invert the conductivity type of said invertible channel; said gate contact containing a P type conductivity material [of the other of the conductivity [types]; said vertical invertible channel material having a constant concentration along its full length.

3. (Amended) The power MOSFET of claim 1 wherein said invertible channel material is epitaxially deposited silicon.

4. (Twice Amended) A power MOSFET comprising, in combination; a P type substrate[of one of the conductivity types]; an epitaxially deposited N type layer [of the other conductivity type] deposited atop said substrate and having a substantially constant concentration; a plurality of spaced trenches having vertical walls extending through said epitaxial layer; a thin gate oxide on said vertical walls and conductive P type polysilicon [of said one of the conductivity types] deposited into said trenches to define a polysilicon gate; a P type source region [of said one conductivity type] formed adjacent the walls of each of said trenches and diffused into the top of said epitaxial layer; a source contact connected to at least said source regions; a drain contact connected to said substrate; whereby said MOSFET has a reduced on resistance.

9. (Twice Amended) A power MOSFET having reduced on resistance comprising, in combination; a P type conductivity substrate; an epitaxially deposited N type conductivity layer [of the other conductivity type] deposited atop said P type substrate to form an epitaxial layer having a substantially constant concentration throughout its volume; a plurality of spaced trenches having vertical walls extending through said epitaxial layer; a thin gate oxide on said vertical walls and conductive polysilicon with a P type conductivity deposited into said trenches to define a polysilicon gate; a P type concentration source region formed adjacent the walls of each of said trenches and diffused into the top

of said epitaxial layer; a source contact connected to at least said source regions; and a drain contact connected to said substrate.

20. (Amended) A trench-type power MOSFET according to claim 1, further having [a] highly doped contact regions at a top portion of said vertical invertible channel.